UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/859,570	05/16/2001	David Chaimers Schie	023P2328	4094

23504 7590 09/25/2002

WEISS & MOY PC
4204 NORTH BROWN AVENUE
SCOTTSDALE, AZ 85251

EXAMINER
VY, HUNG T

ART UNIT	PAPER NUMBER
2828	

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/859,570	SCHIE, DAVID CHAIMERS	
	Examin r	Art Unit	
	Hung T Vy	2828	

-- Th MAILING DATE of this communication app ars on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-50 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-5,9-12,17-19,23-30,33,34,37-40,42,43,45-48,50 is/are rejected.

7)☒ Claim(s) 6-8,13-16,20-22,31,32, 35,36,41,44,49 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Paul Ip

PAUL IP
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In response to the communications dated 01/26/2001 through 05/22/2001, claims 1-50 are pending in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

Information Disclosure Statement (IDS) filed on 05/16/2001 and made of record as Paper No. 2.

Specification

3. The specification has been checked to the extent necessary to determine the presence of possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-6, 9-12, 17-20, 23-30, 33-34, 37-40, 42, 43, 45-48 and 50 are rejected under 35 U. S. C. § 102 (b) as being anticipated by King et al., U.S. patent No. 5,812,572.

Regarding claims 1-3, 9, 12-13,17-19,23,28-30,37-40, 45-48 King et al. disclose a circuit for controlling a laser diode, comprising: a bias circuit (30) coupled to said laser

diode (36) for setting a DC operating point of said laser diode; an amplifier (54) having an output coupled to said laser diode (36) for superimposing an AC signal on said DC operating point, wherein said amplifier has a control input for controlling a maximum output swing of said amplifier; a control circuit (42,44,46,47,52,56) coupled to said control input (10) for setting said maximum output swing; It is inherent that circuit having an adjustable response whereby a transition time of said AC signal may be adjusted because King et al. disclose duty cycle reference (See column 2, line 57-58), control circuit comprises a second amplifier(46 and 54) and a programmable memory (50) coupled to said control circuit for storing values for controlling said maximum output swing (See Fig 1). Programmable memory is an one-time-programmable memory and electrically erasable memory (50) (See Fig 1 and column 7, line 39, 40). The circuit comprises a bias resistor (47) (see column 8, line 12 and fig. 1). The integrated circuit, further comprising: a control circuit (42,44,46,47,52,56) coupled to a third one electrical connections for coupling an output of an external modulation amplifier for supplying an AC modulating signal to said laser diode (36) through a fourth one of said electrical connections, said control circuit having an adjustable response whereby a transition time (10) of said AC signal may be adjusted; and a programmable memory coupled to said control circuit for setting said transition time (see Fig 1).

Regarding claims 4, and 5, King et al. disclose control circuit comprises a current source (44) coupled to said programmable memory and having an output coupled to said control input of said amplifier (46) for providing control of said maximum output swing in response to settings within said programmable memory (50). Programmable

memory is a analog memory, and wherein said current source comprises a voltage controlled current source (44) having an input coupled to an output of said analog memory (50) and an output coupled to said amplifier (46) for controlling said maximum output swing.

Regarding to claims 33-34, and 50, King et al. disclose the integrated circuit, comprising a power on reset circuit for preventing operation of said bias control circuit until an initialization time has elapsed (See column 15, line 59-60).

Regarding to claims 42-43, King et al. disclose the circuit, wherein said programmable memory (50) is an analog memory and wherein said bias circuit further comprises a transistor (20) having a gate coupled to an output of said analog memory for producing a resistance for controlling said bias circuit in conformity with values stored within said analog memory (See fig 1). It is inherent that bias circuit further comprises a voltage controlled current source (44) coupled to said monitor diode (36) including a resistor having thermal resistance variation characteristics matched to thermal resistance variation characteristics (See Fig 1).

With respect to claims 10, 11, and 24 -27, the methods of operating a laser are considered as product by process steps.

Allowable Subject Matter

6. Claims 7-8, 13-16,20-22,31-32,35-36,41, 44, and 49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior art of record and considered pertinent to the applicant's

disclosure does not teach or suggest the claimed limitations. King et al., taken individually or in combination, do not teach the claimed invention having **a digitally programmable current source** comprises: a plurality of current sources, a plurality of switches, a shift register and having **programmable capacitor array** comprises: a plurality of capacitors, a plurality of switches and shift register. King et al. also do not teach the claimed having **under-voltage lockout circuit, a band gap reference, a programmable resistor array.**

Citation of Pertinent References

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The patent to Kuo et al. disclose Method and Apparatus for controlling the wavelength of a leser, U.S. Patent No. 6,222,861.

The patent to Patterson discloses Laser Bisa current Stabilization for Burst Mode Fiber Optic Communication System, U.S. Patent No. 4,709,416.

Conclusion

8. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung VY whose telephone number is (703) 605-0759. The examiner can normally be reached on Monday-Friday 8:30 am - 5:30pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul IP can be reached on (703) 308-3098. The fax numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

10. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PAUL IP
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Hung T. Vy
Art Unit 2828

September 20, 2002